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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,846	07/08/2003	Hector Torres	TI-35321	9187

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Dan Swayze
Texas Instruments Incorporated
M/S 3999
P.O. Box 655474
Dallas, TX 75265

EXAMINER	
WELLS, KENNETH B	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,846	TORRES, HECTOR	
	Examiner	Art Unit	
	Kenneth B. Wells	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

On line 1 of the abstract, the phrase "The present invention discloses" should be changed to --A--. Also, the legal terminology "comprising" should be removed and replaced with --including--.

2. The drawings are objected to because in Fig. 2, it cannot be determined which elements form the voltage regulator 24 (because the arrow is only pointing from the reference numeral to the drain of FET MP1). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. Claims 11, 12 and 16 are objected to because of the following informalities: the comma on line 2 of claim 11 is grammatically improper and should therefore be deleted. In claim 12, "a transistor" lacks clear antecedent basis because plural transistors have been previously recited and it cannot be determined if this is a further transistor, or if it is referring to one of the previously recited transistors. In claim 16, line 5, "current" should be made plural.

4. Claims 1-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "dynamic current switch" is vague and indefinite. This is not a term of art, and applicant has not clearly defined it in the specification or the claims, Thus, it cannot be determined what structure is necessary to meet this limitation (i.e., just a pair of FETs such as FETs MN3 and MN4 in instant Fig. 2? Or just one of them? Or both of them and also another transistor such as BJT Q5? Would the transistors need to be connected to some type of specific control inputs?)

In claim 3, it cannot be determined what is meant by "voltage regulator" because of the above-noted problem with the drawings, and also because the specification does not clearly define what elements of the invention (if any) form the voltage regulator.

In claim 17, it makes no sense to recite one of the second pairs of transistors being "high" because transistors are not high or low, only nodes are.

Claim 25 is also indefinite because it makes no sense to recite the two last steps separately since they are the same step, i.e., if the tri-state switches are part of the dynamic

current switch, then once current is conducted through one tri-state switch it will inherently be also conducted through the dynamic current switch.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 13-15 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Urakawa et al.

As to claim 1, note Fig. 6, where the recited "differential first pair of transistors" reads on BJT's Q2 and Q3; the recited "voltage drive stage" reads on BJT's Q8 and Q9; the recited "first pair of nodes" reads on the collectors of Q2, Q3; the recited "second pair of nodes" reads on the emitters of Q8, Q9; and the recited "dynamic current switch" (to the extend understood) reads on the combination of Q10, Q11 and current source I5.

As to claim 2, the recited resistors read on R1 and R2 of Urakawa et al's Fig. 6 circuitry.

As to claims 13, 14 and 17, the recited operation is seen to be inherent in Urakawa et al's Fig. 6 circuitry.

As to claim 15, the recited pair of input nodes read on the nodes which receive signals B and V1.

6. Claims 17-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Thompson et al.

As to claim 17, note Fig. 3, where the recited "differential first pair of transistors" reads on BJT's 12 and 14; the recited "voltage drive stage" reads on BJT's 26 and 28; the recited "first pair of nodes" reads on nodes A and B; the recited "second pair of nodes" reads on the emitters of BJT's 26 and 28; and the recited "dynamic current switch" (to the extend understood) reads on the combination of current sources 27 and 29. The recited load resistor reads on either one of resistors 64 or 66.

The limitations of claims 18-24 are deemed to be inherent in the operation of Thompson et al's Fig. 3 driver circuitry.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-12, 16 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urakawa et al.

As to claim 3, the use of voltage regulators in integrated circuits is old and well-known in the art for obtaining well-known benefits (of which fact official notice is taken by the examiner). Thus, claim 3 does not distinguish patentably over Urakawa et al.

The same is true for claims 4 and 5, since load resistors are also notoriously old and well-known in the art (put into the legs of differential stages for the well-known purpose of current limiting).

As to claims 6 and 7, the output voltage is the differential signal D, /D and the output nodes are the nodes which receive these voltage signals.

Claims 8 and 11 also fail to define patentable subject matter over Urakawa et al because making the three current sources I1, I2 and I5 using a serial connection of a resistor and transistor would have been obvious to any person having ordinary skill in the art because (1) the claimed structure is

old and well-known and (2) there is motivation to use such a structure for each of the generic current sources taught by Urakawa et al (i.e., to obtain the well-known advantages of such well-known structures). The input node of claim 8 reads on the node receiving signal A in Urakawa et al's Fig. 6 circuitry.

As to claims 9 and 10, note that all points in the circuit of Urakawa et al are electrically connected to each other either directly or through intervening circuit elements.

In claim 12, the recited transistor reads on BJT Q1 in Urakawa et al's Fig. 6 circuitry.

As to claims 16, 25 and 26, the recited load resistor (which can be interpreted to mean a resistor in one or more of the legs of the differential stages of Urakawa et al's Fig. 6 circuitry) would have been obvious for the reason noted above with regard to claims 4 and 5.

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8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Note Fig. 2 of Carvajal et al which is seen to anticipate each of the independent claims of the instant application (see the discussion of load resistor RLOAD which corresponds to applicant's load resistor RL). Note also the load resistors in the legs of the differential pairs in Aizawa (which can be

interpreted as the recited load resistors of the claims, as noted above).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth B. Wells
Primary Examiner
Art Unit 2816

May 14, 2004